REMARKS

The present Amendment amends claims 1 and 18 and leaves claims 2-8, 11, 12, 17 and 19-29 unchanged. Therefore, the present application has pending claims 1-8, 11, 12 and 17-29.

In the Office Action the Examiner rejected claims 1, 5, 8, 11, 17, 18, 22, 23, 26 and 27 under 35 USC §103(a) as being unpatentable over Tanabe (U.S. Patent No. 5,752,272) in view of Johnson (U.S. Patent No. 5,761,137); rejected claims 2, 19 and 20 under 35 USC §103(a) as being unpatentable Tanabe, Johnson in view of Genduso (U.S. Patent NO. 5,778,422); rejected claims 3, 4 and 21 under 35 USC §103(a) as being unpatentable over Tanabe, Johnson and Conary (U.S. Patent No. 5,935,253); rejected claims 12 and 18 under 35 USC §103(a) as being unpatentable over Tanabe, Johnson, Genduso and Handy (book entitled: "The Cache Memory Book"); and rejected claims 6 and 24 under 35 USC §103(a) as being unpatentable over Tanabe, Johnson and Suzuki (U.S. Patent No. 5,381,532). These rejections are traversed for the following reasons. Applicants submit that the features of the present invention as now more clearly recited in the claims are not taught or suggested by Tanabe, Johnson, Genduso, Conary, Handy and Suzuki whether taken individually or in combination with each other as suggested by the Examiner. Therefore, Applicants respectfully request the Examiner to reconsider and withdraw these rejections.

Amendments were made to independent claims 1 and 18 so as to more clearly describe features of the present invention. Particularly, amendments were made to these claims to more clearly recite that the present invention is directed to a

structure for prefetching data between a processor and memory wherein a first bus is provided for the transfer of instruction codes and a second bus is provided for the transfer of operand data. These features of the present invention allows for the independent transfer of operand data to the processor while prefetching instruction codes. Thus, the present invention can efficiently transfer instruction codes and operand data, for example, in parallel.

The above described features of the present invention are not taught or suggested by any of the references of record whether taken individually or in combination with each other.

Tanabe discloses the prefetching of data from memory in an information processing apparatus. However, Tanabe as acknowledged by the Examiner does not teach or suggest the use of two different buses wherein a first of the buses transfers instruction codes and a second of the buses transfers operand data as in the present invention.

The above noted deficiencies of Tanabe are not supplied by any of the other references of record, particularly Johnson. Johnson merely discloses the general structure of a processor 12, memory 14 and memory controller 22. In the Office Action the Examiner appears to consider that control 16 is a bus for transfer of instruction codes and data bus 20 is a bus for the transfer of operand data. Based on such alleged teachings the Examiner concludes that it would be easy to combine the teachings of Tanabe in view of the teachings in Johnson. However, the Examiner seems to completely mis-understand and mis-describe the teachings of Johnson.

In Johnson, the control bus 16 is a bus in which instruction information is transferred between the processor 12 and the memory controller 14 so as to control the memory 22. Thus, the instruction information being transferred on the control bus 16 are merely control signals, not instruction code to control the operation of memory controller 14. these control signals as per Johnson are instruction codes that are prefetched from the memory as in the present invention. According to the present invention, the instruction codes are stored in memory and the first bus is used to prefetch such instruction codes from memory. Such is clearly not taught or suggested by Johnson.

Further, in Johnson, the data bus 20 is simply for transferring data. However, the data bus 20 as taught by Johnson is not combined with another bus whose use is to prefetch instruction codes as in the present invention.

Thus, as is quite clear from the above, both Tanabe and Johnson suffer from the same deficiencies relative to the features of the present invention as recited in the claims. Therefore, reconsideration and withdrawal of the 35 USC §103(a) rejection of claims 1, 5, 8, 11, 17, 18, 22, 23, 26 and 27 as being unpatentable over Tanabe and Johnson is respectfully requested.

The above noted deficiencies of Tanabe and Johnson are not supplied by any of the other references of record. Particularly, the above described features shown above not to be taught or suggested by Tanabe or Johnson are not taught or suggested by Genduso, Conary, Handy and Suzuki. Thus, combining Tanabe and Johnson with one or more of Genduso, Conary, Handy and Suzuki would still fail to

teach or suggest the features of the present invention as now more clearly recited in the claims.

Accordingly, reconsideration and withdrawal of the other rejections of the claims under 35 USC §103(a) based on the combination of Tanabe and Johnson with one or more of Genduso, Conary, Handy and Suzuki is respectfully requested.

The remaining references of record have been studied. Applicants submit that they do not supply any of the deficiencies noted above with respect to the references utilized in the rejection of claims 1-8, 11, 12 and 17-29.

In view of the foregoing amendments and remarks, Applicants submit that claims 1-8, 11, 12 and 17-29 are in condition for allowance. Accordingly, early allowance of claims 1-8, 11, 12 and 17-29 is respectfully requested.

To the extent necessary, the applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, or credit any overpayment of fees, to the deposit account of Antonelli, Terry, Stout & Kraus, LLP, Deposit Account No. 01-2135 (500.36683CX1).

Respectfully submitted,

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